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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,338	03/31/2004	Ross Stenfort	ADAPP269	8827

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EXAMINER	
MISIURA, BRIAN THOMAS	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,338	STENFORT ET AL.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-20* is/are rejected.

7)☒ Claim(s) *8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The examiner would like to note that an attempt to reach Kenneth Wright at (408) 774-6914 to request an interview was made on Friday July 14. A voicemail was left but never returned. A second attempt to reach Mr. Wright was made on Wednesday July 19. An interview was being requested in an attempt to clear up the interpretation of 'wired endian format' of the examiner, which appears to be different than that of the applicant.

Response to Arguments

Applicant's arguments filed 5/2/2006 have been fully considered but they are not persuasive.

In the applicants arguments, he states that Herz (U.S. PN. 6,965,956) does not teach wired endian logic configured to interface a wired endian format with each of a big endian format of a SAS protocol device and a little endian format of a SATA protocol device. The applicant would like to point out his interpretation of 'wired endian format' based on the applicants disclosed specification. Paragraph **[0014]** of the specification states that: "the wired endian format requires multi-byte values be maintained in transmit order." In paragraph **[0017]** of the specification, the transmit order is defined as: "The transmit order of the four byte dword sequence is defined to begin with a lowest memory address associated with the dword and progress consecutively through the remaining memory addresses associated with the dword." Therefore, wired endian format is defined as a format in which addresses are stored, starting with a lowest memory address associated with a dword, in the order in which they will be transmitted. Based on this definition, a wired endian format will either: for SAS protocol devices using little endian format, store the least significant byte/bit in the lowest memory address or for SATA protocol devices using big endian format, store the most significant byte/bit in the lowest memory address. In conclusion, the examiner fails to see the

difference between wired endian format and either little or big endian format. Therefore, any of the applicants arguments stating that a cited reference has failed to teach 'wired endian format' is considered moot since 'wired endian format' simply appears to be either big or little endian format.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Herz et al. U.S. Patent No. 6,965,956.

2. Per claim 1, Herz discloses: an apparatus defined to communicate electronically with each of a Serial Attached SCSI (SAS) protocol device and a Serial ATA (SATA) protocol device, comprising:

- a phy configured to connect the apparatus to each of the SAS protocol device and the SATA protocol device (column 5 lines 31-43, figure 2 numerals 80 and 34);
- wired endian logic configured to communicate through the phy, the wired endian logic configured to interface a wired endian format of the apparatus with each of a big endian format of the SAS protocol device and a little endian format of the SATA protocol device; and internal circuitry configured to operate in accordance with the wired endian format (column 4 lines 16-28 figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herz et al. U.S. Patent No. 6,965,956 in view of Brune et al U.S. Patent No. 6,622,187.

4. Per claim 2, Herz does not disclose: wherein the internal circuitry configured to operate in accordance with the wired endian format is defined to store and process a sequence of bytes in transmit order.

However, Brune discloses: wherein the internal circuitry configured to operate in accordance with the wired endian format is defined to store and process a sequence of bytes in transmit order (column 7 lines 22-52, figure 7a).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Brune into the system of Herz since both SAS and SATA devices are designed to operate using big and little endian formats respectively.

5. Per claim 3, Herz does not disclose: wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes.

However, Brune discloses: wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes (column 7 lines 22-52, figure 7a).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Brune into the system of Herz since the 4 byte (32 bit) is a common addressing mode and transmitting in sequential order will help with keeping consistent data.

6. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herz et al. U.S. Patent No. 6,965,956 in view of Brune et al U.S. Patent No. 6,622,187, in further view of Crawford et al. U.S. Patent No. 5,948,099.

Per claim 4, Brune discloses:

- discrimination circuitry defined to identify a sequence of bytes in wired endian format as one of a control sequence of bytes and a data sequence of bytes (column 6 lines 25-29, figure 5 numeral 30),
- data sequence processing circuitry defined to convert the data sequence of bytes from the wired endian format to a native format associated with a device to which the data sequence of bytes is to be transmitted (column 6 lines 15-41 figure 5),
- the data sequence processing circuitry also being defined to perform pre-transmission processing on the data sequence of bytes while in native format (column 8 lines 26-40),
- transmission circuitry defined to transmit the sequence of bytes in wired endian format (column 6 lines 29-32, figure 5).

Crawford discloses: the data sequence processing circuitry being further defined to convert the data sequence of bytes from the native format back to the wired endian format upon completion of pre-transmission processing (column 2 lines 56-60).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Brune and Crawford into the system of Herz since the 4 byte (32 bit) is a common addressing mode and transmitting in sequential order will help with keeping consistent data.

7. Per claim 5, Herz discloses: an apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 4, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive (column 2 lines 61 – column 32 figure 1).

8. Per claim 6, Herz does not disclose: wherein the data sequence processing circuitry is defined to represent the native format as the big endian format for the SAS protocol device and the little endian format for the SATA protocol device.

However, Brune discloses: wherein the data sequence processing circuitry is defined to represent the native format as the big endian format for the SAS protocol device and the little endian format for the SATA protocol device (column 6 lines 15-41 figure 5).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Brune into the system of Herz since both SAS and SATA devices are designed to operate using big and little endian formats respectively.

9. Per claim 7, Herz does not disclose: an apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 4, wherein the pre-transmission processing includes cyclic redundancy check data generation and scrambling of the data sequence of bytes.

However, Brune discloses: wherein the pre-transmission processing includes cyclic redundancy check data generation (column 1 lines 58) and scrambling of the data sequence of bytes (column 6 lines 16-24 figure 5, the re-ordering of the bytes can be considered a form of scrambling).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Brune into the system of Herz because a CRC is a good method to make sure the correct data is being transmitted from point to point.

10. Claims 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune et al U.S. Patent No. 6,622,187, in view of Crawford et al. U.S. Patent No. 5,948,099.

11. Per claim 11, Brune discloses: a method for operating a wired endian device to perform a transmission operation, comprising:

- identifying a sequence of bytes to be transmitted as one of a control sequence of bytes and a data sequence of bytes, the sequence of bytes to be transmitted being maintained in a wired endian format (column 6 lines 25-29, figure 5 numeral 30);
- converting the sequence of bytes having been identified as the data sequence of bytes from the wired endian format to a native format, wherein the native format is associated with a device to which the sequence of bytes is to be transmitted (column 6 lines 15-41 figure 5);
- processing the data sequence of bytes in the native format, wherein the processing includes generating cyclic redundancy check data (column 1 lines 58) and scrambling the data sequence of bytes (column 6 lines 16-24 figure 5, the re-ordering of the bytes can be considered a form of scrambling);
- transmitting the sequence of bytes in accordance with the wired endian format (column 6 lines 29-32, figure 5).

Brune does not disclose: converting the data sequence of bytes from the native format to the wired endian format.

However, Crawford discloses: converting the data sequence of bytes from the native format to the wired endian format (column 2 lines 56-60).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Crawford into the system of Brune since one would want to have the address returned to its starting format.

12. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune et al U.S. Patent No. 6,622,187, in view of Crawford et al. U.S. Patent No. 5,948,099, in further view of Herz et al. U.S. Patent No. 6,965,956.

13. Per claim 12: Neither Brune nor Crawford disclose a method for operating a wired endian device to perform a transmission operation as recited in claim 11, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive.

However, Herz discloses: a method for operating a wired endian device to perform a transmission operation as recited in claim 11, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive (column 2 lines 61 – column 32 figure 1).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Herz into the system of Brune and Crawford because a sequence of bytes will always be present and is an effective way to determine an endian format to be used in a system.

14. Per claim 13, Brune discloses: wherein the internal circuitry configured to operate in accordance with the wired endian format is defined to store and process a sequence of bytes in transmit order (column 7 lines 22-52, figure 7a).

15. Per claim 14, Brune discloses: wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes (column 7 lines 22-52, figure 7a).

Per claim 15, please refer to above rejection regarding claim 6.

16. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune et al U.S. Patent No. 6,622,187, in view of Crawford et al. U.S. Patent No. 5,948,099, in further view of Beigel et al. U.S. Patent No. 6,472,975.

17. Per claim 16, Brune discloses:

- receiving a sequence of bytes in a native format, wherein the native format is associated with a device from which the sequence of bytes was transmitted (column 6 lines 15-41 figure 5);
- identifying the sequence of bytes in the native format as representing one of a control sequence of bytes and a data sequence of bytes (column 6 lines 25-29, figure 5 numeral 30);

Brune does not disclose: processing the data sequence of bytes in the native format, wherein the processing includes unscrambling the data sequence of bytes and generating cyclic redundancy check data.

However, Beigel discloses: processing the data sequence of bytes in the native format, wherein the processing includes unscrambling the data sequence of bytes and generating cyclic redundancy check data (column 10 lines 39-44, figure 9)

Brune does not disclose: converting the sequence of bytes from the native format to a wired endian format.

However, Crawford discloses: converting the sequence of bytes from the native format to a wired endian format (column 2 lines 56-60).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Beigel and Crawford into

the system of Brune since the address would need to be returned to its native format before further communication regarding the address could occur, and making sure the data is consistent.

18. Per claims 17 and 20, please refer to above rejection of claim 6.
19. Per claim 18, please refer to above rejection of claim 13.
20. Per claim 19, please refer to above rejection of claim 14.

Allowable Subject Matter

21. Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Misiura

7/20/2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
7/21/06